PCT

WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 5 : G06F 15/66 | A1

(11) International Publication Number: WO 93/11500

(43) International Publication Date: 10 June 1993 (10.06.93)

(21) International Application Number: PCT/JP92/01559

(22) International Filing Date: 27 November 1992 (27.11.92)

(30) Priority data: 07/798,705 27 November 1991 (27.11.91) US

(71) Applicant: SEIKO EPSON CORPORATION [JP/JP]; 4-1, Nishi-Shinjuku 2-chome, Shinjuku-ku, Tokyo 163 (JP).

(72) Inventors: LENTZ, Derek, J. ; 17400 Phillips Avenue, Los Gatos, CA 95032 (US). YOUNG, Linley, M. ; 12495 Pathos Lane, San Diego, CA 92129 (US).

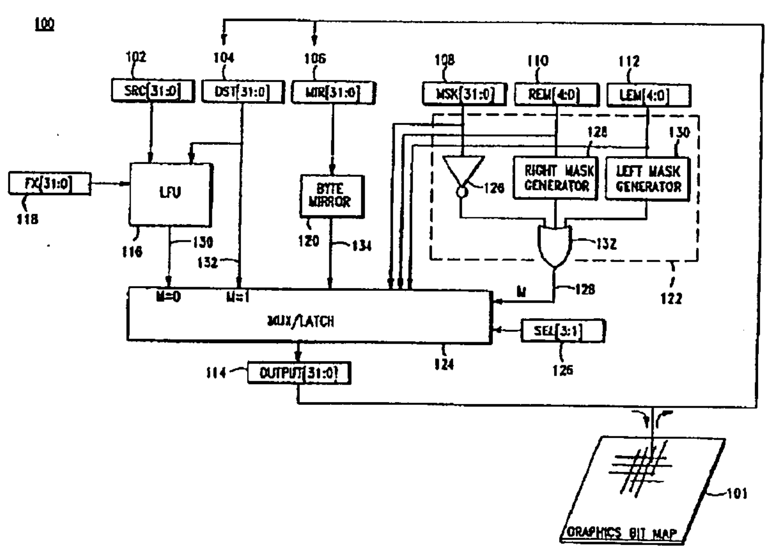
(74) Agents: SUZUKI, Kisaburo et al.; Seiko Epson Corporation, 4-1, Nishi-Shinjuku 2-chome, Shinjuku-ku, Tokyo 163 (JP).

(81) Designated States: JP, KR, European patent (AT, BE, CH, DE, DK, ES, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published
With international search report.

(54) Title: PIXEL MODIFICATION UNIT

(57) Abstract



A pixel modification unit is provided for carrying out a variety of raster graphic manipulations in a RISC graphics processor. The pixel modification unit comprises a logic function unit, a masking unit, and a byte mirror unit. The logic function unit can perform any of 16 different logic operations between each bit of a source operand and a destination operand. The source operand may be a bit map fixed data, while the destination operand is pixel data in the bit map corresponding to the graphics image to be modified. The masking unit can mask any or all bits of a destination operand so that the logic function unit does not operate on the masked bits. When masking is implemented, the output of the pixel modification unit is derived from the masked bits from the destination operand and the unmasked bits which are operated on by the logic function unit. The byte mirror unit horizontally reflects a figure in the bit map via reversing the bit order of data bytes retrieved from the bit map.

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AT	Austria	FR	France	MR	Mauritania
AU	Australia	GA	Gabon	MW	Malawi
BB	Barbados	GB	United Kingdom	NL	Netherlands
BE	Belgium	GN	Guinea	NO	Norway
BF	Burkina Faso	GR	Greece	NZ	New Zealand
BG	Bulgaria	HU	Hungary	PL	Poland
BJ	Benin	IE	Ireland	PT	Portugal
BR	Brazil	IT	Italy	RO	Romania
CA	Canada	JP	Japan	RU	Russian Federation
CF	Central African Republic	KP	Democratic People's Republic of Korea	SD	Sudan
CG	Congo	KR	Republic of Korea	SE	Sweden
CH	Switzerland	KZ	Kazakhstan	SK	Slovak Republic
CI	Côte d'Ivoire	LI	Liechtenstein	SN	Senegal
CM	Cameroon	LK	Sri Lanka	SU	Soviet Union
CS	Czechoslovakia	LU	Luxembourg	TD	Chad
CZ	Czech Republic	MC	Monaco	TG	Togo
DE	Germany	MG	Madagascar	UA	Ukraine
DK	Denmark	ML	Mali	US	United States of America
ES	Spain	MN	Mongolia	VN	Viet Nam
FI	Finland				

51056DOC071673

DESCRIPTION

Title of the Invention: Pixel Modification Unit

Cross-Reference to Related Application

This application is related to a pending patent application entitled, "Single Chip Page Printer Controller," Serial NO. 07/726,929 filed July 8, 1991, which is incorporated by reference as if set forth in full hereinbelow.

Background of the Invention

I. Field of the Invention

The present invention relates to the field of computer graphics and, more particularly, to manipulating data stored in a bit map pertaining to a video image to be presented by a raster printer, screen, display device, or other humanly visible manifestation.

II. Related Art

In raster graphics systems, a graphics image is stored in memory and presented to a printer, screen, or display device by representing the image in the form of a matrix of bits. The matrix is referred to as a "bit map" or a "frame buffer." For monochrome systems, one bit in the bit map represents one visible dot, or picture element (pixel, for short), on the display. For gray scale or color systems, several bits in the bit map represent one pixel or group of pixels on the display.

Many types of graphics processors have been designed and implemented in the art for controlling the display of graphics images. Graphics processors dedicated to this task help relieve the processing burden of the controlling processor. Graphics processors are usually designed to not only generate image data, but also manipulate existing image data in the bit map. Typical graphics manipulations include, for example, rotation and translation. "Rotation" refers to moving an image, or parts thereof, about an axis perpendicular to the display. In contrast, "translation" refers to the linear component of movement, *i.e.*, movement across the display without rotation.

The manipulation of an image requires extensive arithmetic calculations. A reason is that the bit map is dealt with as a coordinate system having an X and a Y component. In order to manipulate a bit in the bit map, both the X and Y components must be considered. In the "X window system," which is an industry standard specification for windowed graphics developed by the Massachusetts Institute of Technology (MIT), Boston, Massachusetts, U.S.A., sixteen

mathematical operations maybe used in order to logically operate upon two operands, such as an X and a Y component representing a pixel.

As a result of the complex mathematics involved in manipulating graphics images, many design techniques have been implemented by those skilled in the art in order to reduce the number of arithmetic gyrations while still providing for manipulation of images. These techniques can be carried out via software, hardware, or combinations thereof. Generally, hardware implementations are faster than software, but their flexibility is more limited.

A well known technique called "masking" has been utilized to reduce the number of requisite mathematical operations when performing image manipulations. Essentially, blocks of pixels are treated as a unit with consideration only to the edge pixels. While the inner pixels of a block are masked from consideration, the number of mathematical operations necessary to manipulate the block is severely reduced. In the art, the transfer of and manipulation of a block of pixels is oftentimes referred to as "bit boundary block transfer" (BitBlt).

Another technique is "clipping." "Clipping" refers to the process of eliminating a portion of an image. Similar to masking, blocks of pixels are treated as a unit with consideration only to edge pixels. Part of an image is clipped away from another part along an edge of pixels, thereby eliminating a portion of the image. Using this procedure, it is not necessary to perform mathematical calculations on pixel data within the area that has been removed.

Still another well known technique for reducing the number of mathematical operations necessary to perform image manipulations is "mirroring." "Mirroring" is used to symmetrically reflect an image, or parts thereof, about an axis, such as a vertical or horizontal axis. The mirroring of data is oftentimes accomplished by sending pixel data through a barrel shifter or like device.

Although the foregoing techniques have to some extent reduced the arithmetic overload associated with performing image manipulations, graphics processors with higher performance and flexibility than those in the past are still needed in the highly competitive graphics industry where speed and efficiency are the primary driving forces.

Summary of the Invention

The present invention is a high performance, pixel modification unit for performing manipulations to bit map data in a graphics processor. The pixel modification unit comprises a logic function unit, a masking unit, and a byte mirror unit.

The logic function unit can perform logic operations on individual bits of two operands referred to as a "source" operand and a "destination" operand. The source operand may be pixel data from a bit map or fixed data, whereas the destination

operand is pixel data from a graphics bit map used by a printer, display device, or the like.

The masking unit can mask any or all bits of a destination operand so that the logic function unit does not operate on the masked bits. When masking is implemented, the output of the pixel modification unit is derived from the masked bits from the destination operand and the unmasked bits which were operated on by the logic function unit. The derivation is provided by a multiplexer unit which is controlled by the masking unit.

The byte mirror unit horizontally mirrors, or reflects, a figure in the bit map via simply reversing the bit order of bytes within pixel data retrieved from the bit map.

The present invention has many advantages. One advantage of the present invention is that bitwise logic operations can be performed on pixel data from a graphics bit map, thereby permitting extreme flexibility in regard to the types of possible logic operations that may be performed. Another advantage is that pixel data may be masked, in whole or in part, thereby allowing for elective manipulation of the bit map. Yet another advantage is that efficient mirroring of an image is provided by simple multiplexing. Still another advantage is that the present invention can be implemented in inexpensive, high performance hardware. Finally, the present invention can be integrated into an integrated circuit (IC), such as a RISC microprocessor. Undoubtedly, other features and advantages of the present invention will become more apparent to one of skill in the art upon examination of the text and the drawings associated herewith.

Brief Description of the Drawings

The present invention, as defined in the claims, can be better understood with reference to the following drawings.

FIGURE 1 illustrates a block diagram of the pixel modification unit in accordance with the present invention; and

FIGURE 2 illustrates a low-level block diagram of the byte mirror unit shown in FIGURE 1.

Detailed Description of the Preferred Embodiment

The architecture of the pixel modification unit 100 in accordance with the present invention is illustrated in FIGURE 1. The pixel modification unit 100 can be implemented in a graphics processor to modify pixel data contained within a graphics bit map 101 (also known in the art as a destination bit map) corresponding to an image to be printed or displayed on a display device. Generally, the pixel modification unit 100 receives various input operands 102-112, which includes a pixel data from graphics bit map 101, performs mathematical manipulations on

these operands, and then provides an output 114, which is pixel data stored back in the graphics bit map 101.

In accordance with the present invention, the pixel data in the graphics bit map may be modified by masking the destination operand 104, byte mirroring of a mirror operand 106, and bitwise logic operations between a source operand 102 and a destination operand 104. In the context of this document, the "mirror" operand 106 and "destination" operand 104 are pixel data from the graphics bit map 101 corresponding to a printer, display device, or the like. On the other hand, the "source" operand 102 is a pixel data from a bit map or fixed data which can be dynamically programmed, for example, by controlling software.

With reference to FIGURE 1, the pixel modification unit 100 comprises a logic function unit (LFU) 116, a byte mirror unit 120, a masking unit 122, and a multiplexer (MUX/LATCH) 124.

In the preferred embodiment, the logic function unit 116 latches a 32-bit source (SRC) operand 102 and a 32-bit destination (DST) operand 104. The byte mirror unit 120 latches a 32-bit mirror (MIR) operand 106, which is essentially a destination operand to be horizontally mirrored, or reflected. The masking unit 122 latches a 32-bit mask (MSK) operand 108, a 5-bit right edge mask (REM) operand 110, and a 5-bit left edge mask (LEM) operand 112. The interrelation of the foregoing mask operands will be discussed in further detail below. The multiplexer 124 selects and latches the outputs of the logic function unit (LEU) 116, the byte mirror unit 120, or the masking unit 122 so as to provide the 32-bit output 114.

The logic function unit 116 can perform any of 16 industry standard logic functions in a bitwise fashion between the source operand 102 and the destination operand 104. The logic operation performed by the logic function unit 116 is determined by the dynamically programmable 4-bit control input FX[3:0] 118. The logic function unit 116 decodes the control input FX[3:0] 118 as indicated in Table A hereafter.

TABLE A	
LFU Operation	FX[3:0]
0	0000
SRC&DST	0001
SRC&~DST	0010
SRC	0011
~SRC&DST	0100
DST	0101
SRC^DST	0110
SRC|DST	0111
~SRC&~DST	1000
~SRC^DST	1001
~DST	1010
SRC|~DST	1011
~SRC	1100
~SRC|DST	1101
~SRC|~DST	1110
1	1111

The masking unit 122 comprises a logic invertor 126, a right mask generator 128, a left mask generator 130, a combiner 132, which is merely an OR logic function in the preferred embodiment. The logic invertor 126 inverts the bits of the mask operand 108 and is merely a design specific detail in the preferred embodiment. The invertor 126 is used to set the polarity of the mask data which in turn allows the pixels to be modified, but need not be implemented in order to accomplish the features of the present invention. Moreover, the right and left mask generators 128, 130 decode the REM operand 110 and the LEM operand 112, respectively, in order to mask the destination operand 104. In other words, these operands are used to determine which bits will be unchanged by the logic function unit 116. The outputs from the right and left mask generators 128, 130 in response to the respective values of the REM and LEM operands 110, 112 are shown below in respective Tables B and C.

TABLE B	
REM [4:0]	Right Generator Output [31:0]
00000	11111........1110
00001	11111........1100
00010	11111........1000
.	.
.	.
11111	00000........0000

51056DOC071678

TABLE C	
LEM [4:0]	Left Generator Output [31:0]
00000	00000........0000
00001	00000........0001
00010	00000........0011
.	.
.	.
11111	01111........1111

As indicated in FIGURE 1, the outputs from the right and left mask generators 128, 130 are combined with the inversion of the mask operand 108 by the combiner 132. The outcome of this combining function, denoted by reference numeral 128, determines whether original bits 132 of the destination operand 104, or alternatively, modified bits 130 of the destination operand 104 are passed through the multiplexer 124 to the output 114.

For further clarification of bitwise operations in accordance with the present invention, consider the following example. Consider the scenario when all bits of the destination operand 104 are to be modified. In such case, the output 114 will be the result of LFU operation on all 32-bits of the original destination operand 104. The bits comprising the output 114 are outputted from LFU 116 as indicated by reference arrow 130. In order to accomplish the desired effect, all bits 128 from the masking unit 122 must be at a logic low (M=0). A possible combination of masking operands 108, 110, 112 would be as follows: MSK[31:0]=11 ... 111, REM[4:0]=11111 and LEM[4:0]=00000.

As another example, consider the case when only the bits 3-27 of the destination operand 104 wish to be modified. A possible combination of mask operands 108, 110, 112 which could achieve this result is as follows: MSK[31:0]=0000111 ... 1000, REM[4:0]=11111, and LEM[4:0]=00000. Another possible combination resulting in the same functionality would be as follows: MSK[31:0]=1111 ... 1111, REM[4.0]=11011, and LEM[4.0]=00011. Hence, it is apparent that many combinations of the mask operands 108, 110, 112 can result in the same ultimate masking operation.

The horizontal mirroring of images, or parts thereof, is another important feature of the present invention. The byte mirror unit 120 reverses the bit order of each byte (4 bytes = 1 word) within each mirror operand 106, which is essentially a data word having 4 data bytes. The mirrored word is sent to the multiplexer 124, as indicated by a reference arrow 134.

A low level block diagram of the byte mirror unit 120 is illustrated in FIGURE 2. In accordance with the preferred embodiment, byte mirroring involves simply crossing logic paths or wires. Consequently, it is easy to implement and is reliable. Byte mirroring is sufficient added support for horizontal mirroring of bit

map images in most instances because different data sizes, such as 2 and 4 bytes, can be mirrored on a byte basis, and bytes can be swapped with other conventionally available hardware.

Referring to FIGURE 2, a 32-bit word input MIR[31:0] 106 comprising four data bytes 204, 206, 208, 210 is operated upon by the byte mirror unit 120 so as to reverse the order of bits within each byte, as collectively indicated by a reference numeral 212. For example, the byte located in the most significant position of the word input 106, denoted by reference 204, is transformed into a byte 214 which still resides in the most significant position of the word input 106, but has been transposed to reverse bit order.

Referring again to FIGURE 1, the multiplexer 124 can output any of the following: the mirror operand 106, the mask operand 108, the REM operand 110, the LEM operand 112, or the modified destination operand (LFU output) 130. The multiplexer 124 is controlled by the output 128 of the masking unit 122 and also by a dynamically programmable select register 126. The select register 126 is decoded into read enables for the multiplexer 124.

Although the preferred embodiment of the present invention has been described in detail above, those skilled in the art will readily appreciate the many additional modifications and applications that are possible without materially departing from the novel teachings of the present invention. For example, in the preferred embodiment, only one bit in the bit map 101 corresponds to a pixel, because the pixel modification unit 100 is envisioned for a black/white printer. However, the principles described are equally applicable to grey scale or color printer systems as well as video screen systems. Accordingly, all such modifications and applications are intended to be included within the scope of the present invention as defined within the following claims.

Claims

The following is claimed:

1. A system for bitwise manipulation of raster graphics data, comprising:

logic function means for performing a bitwise logic operation between a source operand and a destination operand to generate a modified destination operand, said source operand being either fixed data or a secondary bit map, said destination operand being a primary bit map corresponding to an image to be manipulated;

a masking means for preventing said logic function means from operating on one or more bits of said destination operand; and

multiplexer means controlled by said masking means, said multiplexer means for providing an output from said modified destination operand and said destination operand.

2. The system of claim 1, wherein said masking means comprises a right mask generator, a left mask generator, and a combiner, said right and left mask generators for providing a respective right and left mask output for defining a respective right and left mask, said combiner for logically combining said right and left mask outputs with a mask operand for controlling said multiplexer means.

3. The system of claim 1, further comprising a byte mirror means for moving bit map data forming a figure in said image so that said figure is horizontally reflected in said image.

4. The system of claim 2, wherein said combiner performs a logic OR function.

5. The system of claim 3, further comprising a means for reversing the order of bits within each byte of an inputted mirror operand so as to effectuate said reflection.

6. A method for providing pixel modification of an image in a graphics processor, the method comprising the steps of:

performing bitwise logic operations between a source operand and a destination operand in order to provide a modified destination operand, said source operand being either fixed data or a secondary bit map, said destination operand being a primary bit map corresponding to said image;

determining which bits of said destination operand are to be masked;

providing an output derived from the masked bits from said destination operand and the unmasked bits from said modified destination operand.

7. The method of claim 6, further comprising the steps of:

generating a right mask signal indicating which bits near the most significant position of said destination operand are to be masked;

generating a left mask signal indicating which bits near said least significant position of said destination are to be masked;

combining said right masked signal and said left masked signal along with a mask operand; and

multiplexing the bits of said destination operand and said modified destination operand to derive said output based upon the control of said combiner.

8. The method of claim 6, further comprising the step of reversing the order of bits within each byte of a second destination operand so as to reflect a figure horizontally.

9. The method of claim 6, further comprising the step of selecting one of sixteen logic functions to be performed in bitwise fashion between said source operand and said destination operand.

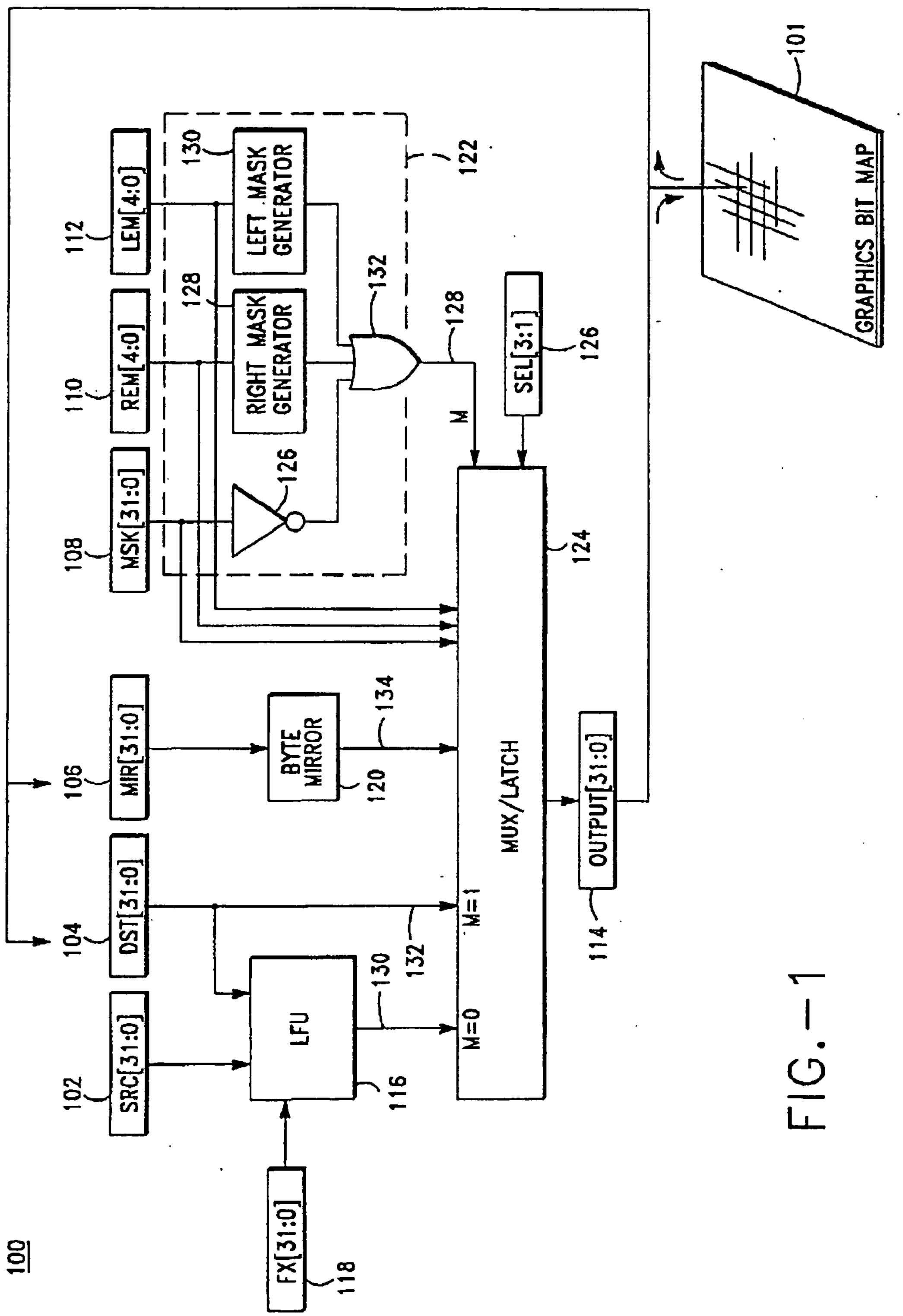

100
SRC[31:0]
102
DST[31:0]
104
MIR[31:0]
106
MSK[31:0]
108
REM[4:0]
110
LEM[4:0]
112
LFU
116
FX[31:0]
118
BYTE MIRROR
120
134
130
132
M=0
M=1
MUX/LATCH
124
OUTPUT[31:0]
114
LEFT MASK GENERATOR
130
RIGHT MASK GENERATOR
128
126
132
128
M
SEL[3:1]
126
122
GRAPHICS BIT MAP
101

FIG.—1

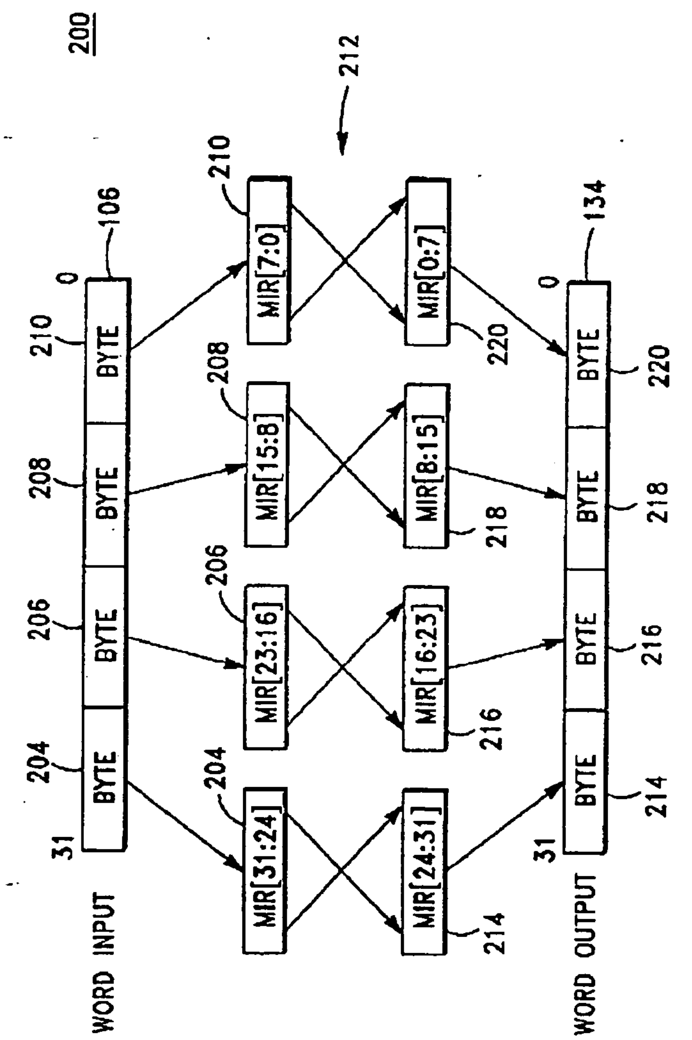

200
212
WORD INPUT
31
0
BYTE
BYTE
BYTE
BYTE
204
206
208
210
106
MIR[31:24]
MIR[23:16]
MIR[15:8]
MIR[7:0]
MIR[24:31]
MIR[16:23]
MIR[8:15]
MIR[0:7]
214
216
218
220
WORD OUTPUT
134

FIG.—2

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP 92/01559

A. CLASSIFICATION OF SUBJECT MATTER

IPC5: G06F 15/66
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC5: G06F G09G

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

WPI, CLAIMS, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	WO, A1, 8605299 (MITSUBISHI DENKI KABUSHIKI KAISHA), 12 Sept 1986 (12.09.86), see the whole document -- --------	1-9

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" erlier document but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance: the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance: the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
15 February 1993	26.02.93
Name and mailing address of the ISA/ European Patent Office, P.B. 5818 Patentlaan 2 NL-2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Authorized officer Jan Silfverling

Form PCT/ISA/210 (second sheet) (July 1992)

51056DOC071685

SA 7117

INTERNATIONAL SEARCH REPORT

Information on patent family members

29/01/93

International application No.

PCT/JP 92/01559

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
WO-A1- 8605299	12/09/86	EP-A- 0216931	08/04/87
		JP-C- 1590806	30/11/90
		JP-B- 2014750	09/04/90
		JP-A- 61199175	03/09/86
		US-A- 4759076	19/07/88

Form PCT/ISA/210 (patent family annex) (July 1992)

51056DOC071686